MARTHANDAM COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. VLSI DESIGN

VLSI & DSP LAB

Equipments Available in the Lab

Sl.No	Hardware	Specification	Quantity
1.	Desktops	Dell Desktop Motherboard 1GB RAM, LED Monitor Zebronics Keyboard and Optical Mouse	15 Nos
2.	Fixed DSP processor TMS 320C50		10
3.	Fixed/floating point DSP processor TMS 320C5416		05
4.	Function Generator		10
5.	CRO		10
6.	LAN Trainer		05
7.	UPS		01
8.	LAN Switch		02
9.	FPGA Trainer kit		15
10.	Xilinx Vertex 4 Boards		02
11.	Altera Cyclone II Boards		04
12.	Embedded trainer kits with ARM board		7
13.	Embedded trainer kits suitable for wireless communication		7
14.	Analog Discovery		10

15.	Digital storage Oscilloscope		7
16.	Interface Board – ADC		2
17.	DAC		2
18.	Motor Control		2
Software			
1	Tanner Software		
2	MATLAB		

COURSES OFFERED

Sl.No	Odd Sem (Course code & Name)	Class	Even Sem (Course code & Name)	Class
1	VL4111 - FPGA Laboratory	I ME	VL4211 - Verification using UVM Laboratory	I ME
2	VL4112 – Analog IC Design Laboratory	I ME		
3	AP4152 - Advanced Digital System Design	I ME		
4	DS4151 - Digital Image and Video Processing	II ME		

DS4151 - DIGITAL IMAGE AND VIDEO PROCESSING LABORATORY

OBJECTIVES:

- To provide the student with basic understanding of image fundamentals and transforms
- To provide exposure to the students about image enhancement and restoration
- To impart a thorough understanding about segmentation and Recognition.
- To know the Video Processing and motion estimation
- Learning the concepts will enable students to design and develop an image processing application .

OUTCOMES

On the successful completion of the course, students will be able to

- Analyze the digital image, representation of digital image and digital images in transform Domain.
- Analyze the detection of point, line and edges in images and understand the redundancy in images, various image compression techniques.
- Analyze the video technology from analog color TV systems to digital video systems, how video signal is sampled and filtering operations in video processing.
- Obtain knowledge in general methodologies for 2D motion estimation, various coding used in video processing.
- Design image and video processing systems.

LIST OF EXPERIMENTS

1. Histogram Equalization
2. Image Filtering (spatial-domain)
3. Image Filtering (frequency-domain)
4. Image Segmentation
5. Familiarization with Video Processing tools
6. Denoising video
7. Video resizing
8. Background subtraction
9. Interpolation methods for re-sampling
10. Adaptive unsharp masking based interpolation for video up-sampling
11. Gaussian mixture model (GMM) based background subtraction
12. Video encoding

AP4152 - ADVANCED DIGITAL SYSTEM DESIGN

OBJECTIVES:

- To design asynchronous sequential circuits.
- To learn about hazards in asynchronous sequential circuits.
- To study the fault testing procedure for digital circuits.
- To understand the architecture of programmable devices.
- To design and implement digital circuits using programming tools.

OUTCOMES

On the successful completion of the course, students will be able to

- Analyse and design synchronous sequential circuits.
- Analyse hazards and design asynchronous sequential circuits.
- Knowledge on the testing procedure for combinational circuit and PLA.
- Able to design PLD and ROM.
- Design and use programming tools for implementing digital circuits of industry standards

LIST OF EXPERIMENTS

1. Design of Registers by Verilog HDL.
2. Design of Counters by Verilog HDL.
3. Design of Sequential Machines by Verilog HDL.
4. Design of Serial Adders , Multiplier and Divider by Verilog HDL.

5. Design of a simple Microprocessor by Verilog HDL.

VL4111 - FPGA LABORATORY

OBJECTIVES:

- To help engineers read, understand, and maintain digital hardware models and conventional verification test benches written in Verilog and System Verilog.
- To provide a critical language foundation for more advanced training on System Verilog

OUTCOMES

On the successful completion of the course, students will be able to

- Understand and use the System Verilog RTL design and synthesis features, including new data types, literals, procedural blocks, statements, and operators, relaxation of Verilog language rules, fixes for synthesis issues, enhancements to tasks and functions, new hierarchy and connectivity features, and interfaces.
- Appreciate and apply the System Verilog verification features, including classes, constrained random stimulus, coverage, strings, queues and dynamic arrays, and learn how to utilize these features for more effective and efficient verification.
- The implementation of higher level of abstraction to design and verification
- Develop Verilog test environments of significant capability and complexity.
- Integrate scoreboards, multichannel sequencers and Register Models

LIST OF EXPERIMENTS

1. Introduction to Verilog and System Verilog
2. Running simulator and debug tools
3. Experiment with 2 state and 4 state data types
4. Experiment with blocking and non-blocking assignments
5. Model and verify simple ALU
6. Model and verify an Instruction stack
7. Use an interface between testbench and DUT
8. Developing a test program
9. Create a simple and advanced OO testbench
10. Create a scoreboard using dynamic array
11. Use mailboxes for verification
12. Generate constrained random test values
13. Using coverage with constrained random tests

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VL4112 - ANALOG IC DESIGN LABORATORY

OBJECTIVES:

- Carry out a detailed analog circuit design starting with transistor characterization and finally realizing an IA design.
- At various stages of design, exposure to state of art CAD VLSI tool in various phases of experiments designed to bring out the key aspects of each important module in the CAD tool including the simulation, layout, LVS and parasitic extracted simulation.

OUTCOMES

On the successful completion of the course, students will be able to

- **CO1:** Design digital and analog Circuit using CMOS given a design specification.
- Design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances

- Use EDA tools for Circuit Design

LIST OF EXPERIMENTS

1. Extraction of process parameters of CMOS process transistors
a. Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
b. Plot ID vs. VGS at particular drain voltage for NMOS, PMOS and determine Vt.
c. Plot log ID vs. VGS at particular gate voltage for NMOS, PMOS and determine IOFF and subthreshold slope.
d. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
e. Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS of appropriate voltage To extract Vth use the following procedure.
i. Plot gm vs VGS using SPICE and obtain peak gm point.
ii. Plot y=ID/(gm) as a function of VGS using SPICE.
iii. Use SPICE to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
f. Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it.
2. CMOS inverter design and performance analysis
a. i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
ii. Plot VTC for CMOS inverter with varying VDD.
iii. Plot VTC for CMOS inverter with varying device ratio.
b. Perform transient analysis of CMOS inverter with no load and with load and determine propagation delay tpHL, tpLH, 20%-to-80% rise time tr and 80%-to-20% fall time tf.
c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.
3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.

4. Single stage amplifier design and performance analysis
a. Plot small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors.
b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
i. Establish a test bench to achieve VDSQ=VDD/2.
ii. Calculate input bias voltage for a given bias current.
iii. Use spice and obtain the bias current. Compare with the theoretical value
iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier
v. using small signal analysis in spice, considering load capacitance.
vi. Plot step response of the amplifier with a specific input pulse amplitude.
vii. Derive time constant of the output and compare it with the time constant
viii. resulted from -3dB Band Width.
ix. Use spice to determine input voltage range of the amplifier
5. Three OPAMP Instrumentation Amplifier (INA). Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
i. Draw the schematic of op-amp macro model.
ii. Draw the schematic of INA.
iii. Obtain parameters of the op-amp macro model such that it meets a given specification for:
i.low-frequency voltage gain,
ii. unity gain BW (fu),
iii.input capacitance,
iv.output resistance,
v. CMRR
d. Draw schematic diagram of CMRR simulation setup.
e. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
f. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
g. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.
6. Use Layout editor.
a. Draw layout of a minimum size inverter using transistors from CMOS process library. Use Metal 1 as interconnect line between inverters.
b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.
c. Extract the netlist. Use extracted netlist and obtain tPHLtPLH for the inverter using Spice.
d. Use a specific interconnect length and connect and connect three inverters in a chain.
e. Extract the new netlist and obtain tPHL and tPLH of the middle inverter.
f. Compare new values of delay times with corresponding values obtained in part ‘c’.
7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter
a. low-frequency voltage gain,
b. unity gain BW (fu),
c. Power dissipation
i. Perform DC analysis and determine input common mode range and compare with the theoretical values.

ii. Perform time domain simulation and verify low frequency gain.
iii. Perform AC analysis and verify.

VL4211 - VERIFICATION USING UVM LABORATORY

OBJECTIVES:

- To help the engineers to design the system with verilog and system Verilog
- Complete understanding of Verilog Hardware Description Language
- to practice for writing synthesizable RTL models that work correctly in both simulation and synthesis.

OUTCOMES

On the successful completion of the course, students will be able to

- Understand the features and capabilities of the UVM class library for system Verilog
- Combine multiple UVCs into a complete verification environment
- Create and configure reusable, scalable, and robust UVM verification components (UVCs)
- Create a UVM test bench structure using the UVM library base classes and the UVM factory
- Develop a register model for your DUT and use the model for initialization and accessing DUT registers

LIST OF EXPERIMENTS

1. Simulate a simple UVM testbench and DUT
2. Examining the UVM testbench
3. Design and simulate sequence items and sequence
4. Design and simulate a UVM driver and sequencer
5. Design and simulating UVM monitor and agent
6. Design, simulate and examine coverage
7. Design and simulate a UVM scoreboard and environment, and verifying the outputs of a (faulty) DUT
8. Design and simulate a test that runs multiple sequence
9. Design and simulate a configurable UVM test environment